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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/779,904 | 02/17/2004 | Masahiro Ishida | 02008.071003 | 9608 |

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OSHA LIANG L.L.P.
1221 MCKINNEY STREET
SUITE 2800
HOUSTON, TX 77010

| EXAMINER | |
|---|---|
| LOUIE, OSCAR A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2136 | |

| MAIL DATE | DELIVERY MODE |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/779,904 | ISHIDA ET AL. | |
| | Examiner | Art Unit | |
| | Oscar A. Louie | 2136 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *4, 16 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4, 16, & 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/04; 06/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This first non-final action is in response to the original filing of 02/17/2004. Claims 4, 16, & 27 are pending and have been considered as follows.

### *Examiner's Note*

1. The Applicant appears to be attempting to invoke 35 U.S.C. 112 6th paragraph in Claims 16 & 27 by using "means-plus-function" language. However, the Examiner notes that the only "means" for performing these cited functions in the specification appears to be either computer program modules or elements of an apparatus non-explicitly cited in the specification. While the claims pass the first test of the three-prong test used to determine invocation of paragraph 6, since no other specific structural limitations are disclosed in the specification, the claims do not meet the other tests of the three-prong test. Therefore, 35 U.S.C. 112 6th paragraph has not been invoked when considering these claims below.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 16, & 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugasawara (US-6043672-A).

Claims 4 & 16:

Sugasawara discloses a fault analysis method & apparatus for presuming a fault location of a semiconductor IC comprising,

- "applying a power supply voltage to said semiconductor IC" (i.e. "A selectable power supply line for providing power to a particular section of the integrated circuit is activated by an enable signal provided to a selectable power supply switch coupled to the selectable power supply line") [column 3 lines 28-32];
- "supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC" (i.e. "Test development strategies include functional test wherein automatic test equipment (ATE) test programs are performed in which the circuit under test is stimulated with specified inputs while the outputs are monitored to determine if they correspond with simulated logic values") [column 1 lines 54-58];
- "the electric potential of which changes in accordance with change of said supplied test pattern, to be corresponding to said test pattern sequence" (i.e. "Test development strategies include functional test wherein automatic test equipment (ATE) test programs

are performed in which the circuit under test is stimulated with specified inputs while the outputs are monitored to determine if they correspond with simulated logic values") [column 1 lines 54-58];

- "measuring a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern" (i.e. "Once halted (i.e., no transistor state switching is occurring) the power supply of the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits") [column 2 lines 14-18];
- "determining whether said transient current shows abnormality or not" (i.e. "the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits. Such quiescent current tests are effective in detecting many faults that would otherwise not be found by other test strategies") [column 2 lines 16-20];
- "presuming a fault location out of said analysis points based on said test pattern sequence" (i.e. "This approach has typically included measuring current in a region of the integrated circuit, cutting lines to sections within the same region other than the section of interest, and then taking a additional measurements of current in the region") [column 2 lines 49-53];
- "where the transient power supply current shows abnormality" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];

- "said transient power supply current is determined to be abnormal in case time integral of said transient power supply current is over a predetermined value in said step of determining" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];

but Sugasawara does not explicitly disclose,

- "storing an analysis point included in said IC"
- "said analysis point stored to be corresponding to said test pattern sequence"

however, Sugasawara does disclose,

- "the resulting value is compared to predetermined reference values or test limits" [column 2 lines 16-18];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "storing an analysis point included in said IC" and "said analysis point stored to be corresponding to said test pattern sequence," in the invention as disclosed by Sugasawara since predetermined reference values or test limits would typically be stored within the testing device in order to be compared to the resulting value(s).

Claim 27:

Sugasawara discloses a fault analysis method & apparatus for presuming a fault location of a semiconductor IC comprising,

- "a means for applying a power supply voltage to said semiconductor IC" (i.e. "A selectable power supply line for providing power to a particular section of the integrated

circuit is activated by an enable signal provided to a selectable power supply switch coupled to the selectable power supply line") [column 3 lines 28-32];

- "a means for supplying a test pattern sequence comprising a plurality of test patterns to said semiconductor IC" (i.e. "Test development strategies include functional test wherein automatic test equipment (ATE) test programs are performed in which the circuit under test is stimulated with specified inputs while the outputs are monitored to determine if they correspond with simulated logic values") [column 1 lines 54-58];
- "the electric potential of which changes in accordance with change of said supplied test pattern, to be corresponding to said test pattern sequence" (i.e. "Test development strategies include functional test wherein automatic test equipment (ATE) test programs are performed in which the circuit under test is stimulated with specified inputs while the outputs are monitored to determine if they correspond with simulated logic values") [column 1 lines 54-58];
- "a means for measuring a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern" (i.e. "Once halted (i.e., no transistor state switching is occurring) the power supply of the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits") [column 2 lines 14-18];
- "a means for determining that said transient current is abnormal in case time integral of said transient power supply current is over a predetermined value" (i.e. "the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits. Such quiescent current tests are effective in detecting

many faults that would otherwise not be found by other test strategies") [column 2 lines 16-20];

- "a means for presuming a fault location out of said analysis point based on said test pattern sequence" (i.e. "This approach has typically included measuring current in a region of the integrated circuit, cutting lines to sections within the same region other than the section of interest, and then taking a additional measurements of current in the region") [column 2 lines 49-53];
- "where the transient power supply current shows abnormality" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];

but Sugasawara does not explicitly disclose,

- "a means for storing an analysis point included in said IC"
- "said analysis point stored to be corresponding to said test pattern sequence"

however, Sugasawara does disclose,

- "the resulting value is compared to predetermined reference values or test limits" [column 2 lines 16-18];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a means for storing an analysis point included in said IC" and "said analysis point stored to be corresponding to said test pattern sequence," in the invention as disclosed by Sugasawara since predetermined reference values or test limits would typically be stored within the testing device in order to be compared to the resulting value(s).

***Conclusion***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2100 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

OAL
08/22/2007

Nasser Moazzami
Supervisory Patent Examiner

8/22/07